AMENDMENTS TO THE CLAIMS

Cancel Claims 1 and 14. Please accept amended Claims 2, 4, 15 and 18 as follows:

1. (Canceled)

2. (Currently Amended) The delay-locked loop of claim [[1]] 19, wherein the delay line is structured such that a unit time delay gradually increases from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

3. (Cancelled)

4. (Currently Amended) The delay-locked loop of claim [[1]] 19, wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

5-14. (Cancelled)

15. (Currently Amended) The circuit of claim [[14]] 19, wherein the delay [[cell]] cells of the delay [[unit]] line have gradually increasing unit time delays from the delay [[cell]] cells of a delay block at [[the]] a front end of the delay [[unit]] line to the delay [[cell]] cells of a delay block at [[the]] a rear end of the delay [[unit]] line.

16-17. (Cancelled)

18. (Currently Amended) The circuit of claim [[14]] 19, wherein the resistance is gradually increased from the delay [[cell]] cells of a delay block of a front end of the delay line to the delay [[cell]] cells of a delay block of a rear end of the delay line.

19. (Previously Presented) A delay-locked loop for receiving an external clock signal and synchronizing a phase of a feedback clock signal with a phase of the external clock signal, the delay-locked loop comprising:

a phase detector for comparing the phase of the external clock signal with the phase of the feedback clock signal and outputting a phase difference as an error control signal;

a delay line, comprising a plurality of delay blocks, each delay block comprising a plurality of delay cells having the same unit time delay, wherein the unit time delay of delay cells from different delay blocks are different, the delay line for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistors of the delay cells from different delay blocks have different resistances and the resistors of the delay cells from the same delay block have the same resistance, to vary the unit time delay; and

a filter unit for generating the shift signal for selecting the number of delay cells in operation in the delay line, in response to the error control signal.